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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 10/601,310 | 06/23/2003 | Masaki Hashimura | T36-156800M/RS | 7969 |
| 21254 | 7590 | 07/19/2005 | EXAMINER | |
| MCGINN & GIBB, PLLC 8321 OLD COURTHOUSE ROAD SUITE 200 VIENNA, VA 22182-3817 | | | LE, DUNG ANH | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2818 | |

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|-------------------------------|----------------------------------|--|
| Office Action Summary | Application No. 10/601,310 | Applicant(s) HASHIMURA ET AL. | |
| | Examiner DUNG A. LE | Art Unit 2818 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-6 and 19-26 is/are allowed.
- 6) ☒ Claim(s) 1, 7, 10 and 12 is/are rejected.
- 7) ☒ Claim(s) 8, 9 and 13-18 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

D6

DETAILED ACTION

Oath/Declaration

The oath/declaration filed on 6/23/2003 is acceptable.

Information Disclosure Statement

This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 6/23/2003 and 5/4/2005 and made of record . The references cited on the PTOL 1449 form have been considered.

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Set of claims 1- 6, refer to Reasons for Indication of Allowable Subject Matter.

Set of claims 7-11

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 7 is rejected under 35 USC 102 (b) as being anticipated by Ikegami et al. (6720522 B2).

Ikegami et al. method of producing a plurality of semiconductor elements by individually dividing semiconductor elements formed on a substrate, said method comprising a step of performing a polishing or blasting process (col 8, lines 65-66) with respect to separation grooves 11T (figs. 4A-4C) after forming said separation grooves by laser beam irradiation (col 9, lines 40-45 and col 15, line 13).

Regarding claims 8- 9 and 11, refer to Reasons for Indication of Allowable Subject Matter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 10 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Ikegami et al. (6720522 B2) in view of the following remark.

Ikegami et al. disclose the claimed invention substrate is made of glass as applied to claim 7, except for substrate is a sapphire substrate. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize sapphire substrate because sapphire is commonly used to prevent undesirable reactions in the contact region, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

Set of claims 12- 18

Claim 12 is rejected under 35 USC 102 (b) as being anticipated by Ikegami et al. (6720522 B2).

Ikegami et al. disclose a method of producing a plurality of semiconductor elements by individually dividing said semiconductor elements formed on a substrate, said method comprising steps of: removing semiconductor layers on parting lines so that (i) only an electrode-forming layer on a side near to said substrate remains on said parting lines or (ii) there is no semiconductor layer on said parting lines; and scanning (fig. 4C, col 10, lines 1-5) said substrate along said parting lines with a laser beam to thereby form broken line-shaped or dot line-shaped separation grooves, wherein said broken line-shaped or dot line-shaped separation grooves formed by laser beam scanning along the parting lines are used so that said substrate is divided into individual semiconductor elements (col 15, lines 12-20).

Regarding claims 13-18, refer to Reasons for Indication of Allowable Subject Matter.

Set of claims 19-26, refer to Reasons for Indication of Allowable Subject Matter .

Reasons for Indication of Allowable Subject Matter

Claims 8- 9, 13- 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Ikegami et al. (U.S. Patent No. 6720522 B2) and Background of Invention, taken individually or in combination, do not teach the claimed invention having **(Regarding claim 8)** separation groove; are formed in a rear surface of said substrate opposite to a front surface of said substrate on which semiconductor layers and electrodes are formed; and said polishing or blasting process is applied to said rear surface; **(Regarding claim 9)** blasting process is used, particles used in said blasting process are selected so that a medium value of diameters of said particles is equal to about a half width of each separation groove, **(Regarding claim 11)** blasting process is used, particles used in said blasting process are mainly of alumina or silicon carbide; **(Regarding claim 13)** wherein the semiconductor layer removal step is carried out by an electrode-forming etching process for exposing an electrode-forming portion of said

electrode-forming layer by etching (Regarding claim 14) wherein in the semiconductor layer removal step, a part of the element-forming surface of said substrate on said parting lines is also removed by dicing; (Regarding claim 15) forming a protective film so that layers formed on a front surface side of said substrate are covered with said protective film before the laser beam scanning step and said protective film can be removed by an after-process; and removing said protective film and unnecessary products produced due to laser beams canning after the -laser beam scanning step; **(Regarding claim 16)** wherein before said separation grooves are used for dividing said substrate into elements, rear grooves corresponding to said parting lines are formed in a rear surface of said substrate; **(Regarding claim 17)** wherein before said separation grooves are used for dividing said substrate into elements, a rear surface of said substrate is polished to reduce a thickness of said substrate so that said substrate can be divided into individual semiconductor elements only by said separation grooves formed in the front surface of said substrate; **(Regarding claim 18)** wherein before said separation grooves are used for dividing said substrate into elements, a rear surface of said substrate is polished to reduce a thickness of said substrate and then rear grooves corresponding to said parting lines are formed in the rear surface of said substrate.

Claims 1- 6 and 19- 26 would be allowed. Claims 1-6 and 19-26 are considered allowable since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Ikegami et al. (U.S. Patent

No. 6720522 B2) and Background of Invention, taken individually or in combination, do not teach the claimed invention having (Regarding claim 1) the steps of scanning said substrate with a laser beam along said parting lines to form separation grooves in a front surface of said substrate; and removing said protective film and unnecessary products produced by said laser beam scanning, wherein said separation grooves formed along said parting lines by said laser beam scanning are used for dividing said substrate into individual semiconductor elements and (Regarding claim 19) step of applying a laser beam on a metal layer formed on said semiconductor wafer and serving as a negative electrode of each of said semiconductor elements to thereby form continuous line-shaped, dot line-shaped, broken line-shaped or cross-shaped separation grooves for separating said semiconductor wafer into said plurality of semiconductor elements.

If Applicants are aware of better art than that which has been cited, they are required to call such to attention of the examiner.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.


A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE 
Primary Examiner
Art Unit 2818